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| 09/957,004 | 09/19/2001 | Kollin Tierling | IMM135 | 2443 |

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PATENT DEPARTMENT (51851)
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| EXAMINER | |
|---|---|
| NGUYEN, NAM V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2635 | |

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/957,004 | TIERLING, KOLLIN | |
| | Examiner | Art Unit | |
| | Nam V. Nguyen | 2635 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 29* is/are rejected.

7)☒ Claim(s) *27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This communication is in response to a request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on November 18 has been entered.

Claims 1-22 and 27-29 are pending.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 6-13,16-17, 19 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson (US# 4,303,907) in view of Kronberg (US# 5,424,731).

Referring to claims 1, 13 and 19, Wilson discloses a switch matrix circuit (i.e. a keyboard sensing circuit) (column 1 lines 38 to 64; see Figure 1) comprising:

A plurality of switches (S11 to S44) (i.e. a key switches) organized in a row (i.e. R1 to R4) and column (i.e. C1 to C4) configuration (column 1 line 47 to 64; see Figure 1); and

A current sensing circuit (20 and 21) (i.e. a current sourcing circuit and current sinking circuit) coupled to the plurality of switches (S11 to S44) (i.e. a key switches) (column 1 line 65 to column 2 line 66; see Figures 1 to 3), the current sensing circuit (20 and 21) including a plurality of resistors (24) each electrically coupled in series with an associated one of the plurality of switches (S11 to S44) (column 2 lines 3 to 18; see Figure 2),

wherein current in the transistor (N2 and N3) in a column is sensed as a logic state indicative of a switch status (i.e. open or closed) of a switch (S11 to S44) within the column (C1 to C4) for a selected row (R1 to R4), and wherein the column (C1 to C4) is configured to conduct at least a threshold current level required for the transistor (N2 and N3) to perform the function if the switch is closed, and to conduct less than the threshold current level if the switch is open, regardless of how many other of the plurality of switches are closed (column 2 lines 3 to column 3 line 61; see Figures 1 to 3).

However, Wilson did not explicitly disclose wherein current amplified by the transistor in a column is sensed as a logic state.

In the same field of endeavor of detecting switch matrix device, Kronberg teaches that current amplified by the transistor (24) in a column is sensed as a logic state (column 4 lines 54 to column 5 line 61; see Figures 3 to 5) in order to detect the peak detection current when a switch is closed.

One of ordinary skilled in the art recognizes using a transistor for current amplification of Kronberg in each of column conductor in a current sinking circuit of Wilson because Wilson

suggests it is desired to use transistors in a current sinking circuit for limiting the current to desired levels (column 2 line 39 to column 3 line 40; see Figures 1-2) and Kronberg teaches a current is determined by the current-regulating device, and the current from the driving circuit flows through the loop and then amplify for detection when a key is pressed normally for a short time (column 3 line 61 to column 5 line 44; see Figures 1 and 5) in order to have a successful and reliable detecting which key was pressed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to use a transistor for current amplification of Kronberg in each of column conductor in a current sinking circuit of Wilson with the motivation for doing so would have been to provide a reliable and valid of sensing a switch status when a switch is pressed.

Referring to Claim 2, Wilson in view of Kronberg disclose the switch matrix circuit of claim 1, Kronberg discloses wherein the transistor further comprises a bipolar junction transistor (column 3 lines 55 to 60; see Figure 1c).

Referring to claim 6, Wilson in view of Kronberg disclose a switch matrix circuit of claim 1, Kronberg discloses wherein a processor (144) (i.e. a host) senses the switch status (column 5 lines 24 to 66; see Figures 5 and 6).

Referring to claims 7-12 and 16-17, Wilson in view of Kronberg disclose a switch matrix circuit and method of claims 1 and 13, the claims 7-12 and 16-17 differ from claim 1 is that the claims 7-12 and 16-17 require the limitation of claim 6 already addressed above and Kronberg

discloses all the limitations to the extent as claimed with respect to claim 6 above, and therefore claims 7-12 and 16-17 are also rejected as being obvious for the same reasons given with respect to claim 1.

Referring to claim 29, Wilson in view of Kronberg disclose the method of claim 13, wherein the row and column configuration comprises a first row and a second row, and wherein detecting the switch status comprises: Scanning the first row (i.e. R1 first) of the switch matrix (12) (i.e. keyblock); and then scanning the second row (i.e. R2) of the switch matrix (12) (i.e. keyblock) (column 2 line 39 to column 3 line 53; see Figure 1).

Claims 3-5 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson (US# 4,303,907) in view of Kronberg (US# 5,424,731) as applied to claim 1, and in further view of Hastreiter (US# 4,667,181).

Referring to claims 3-5 and 19-20, Wilson in view of Kronberg disclose a switch matrix circuit of claim 1, however, Wilson in view of Kronberg did not explicitly disclose a the row and column configuration further comprises an off-diagonal configuration having one switch per row and column intersection in all but one intersection per row.

In the same field of endeavor of scanning switch matrix, Hastreiter discloses a row (11) (i.e. a first plurality of conductors) and column (12) (i.e. a second plurality of conductors) configuration (column 3 lines 30 to 48; see Figure 1) further comprises an off-diagonal configuration having one switch (13) per row (11) and column (12) intersection in all but one

intersection per row (column 3 lines 49 to 59; see Figure 1) in order to connect directly to a data processor which has bi-directional input/output ports.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to recognize to use a switch of a matrix of keyboard conductors that located at each intersection of the conductors except along one diagonal group of intersections of Hastreiter in keypad switch matrix of Wilson in view of Kronberg because having a switch that located at each intersection of the conductors except along one diagonal group of intersections would able to connect directly to a data processor which has bi-directional input/output ports that has been shown to be desirable in the keypad switch matrix circuit of Wilson in view of Kronberg.

Referring to claims 21-22, Wilson in view of Kronberg and Hastreiter disclose a switch matrix circuit of claim 19, Kronberg discloses a diode and resistor circuit for each scan line (column 3 lines 39 to 66; see Figures 1 to 3).

Claims 14-15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson (US# 4,303,907) in view of Kronberg (US# 5,424,731) as applied to claim 13, and in further view of Matsuda (US# 5,151,554).

Referring to claims 14-15, Wilson in view of Kronberg disclose a switch matrix circuit of claim 13, however, Wilson in view of Kronberg did not explicitly disclose further comprising a plurality of resistors each electrically coupled in series with an associated one of the plurality of switches.

In the same field of endeavor of scanning switch matrix, Matsuda discloses a plurality of resistors (i.e. r) each electrically coupled in series with an associated one of the plurality of switches (i.e. sw#1 to sw#9) (column 1 line 24 to 56 and column 2 line 12 to 24; see Figure 1 to 5) in order to connect directly to a data processor which has bi-directional input/output ports.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to recognize to use plurality of resistors each electrically coupled in series with an associated one of the plurality of switches of Matsuda in keypad switch matrix of Wilson in view of Kronberg because having a switch connect series with resistor would improve reliable contact resistance that has been shown to be desirable in the keypad switch matrix circuit of Wilson in view of Kronberg.

Referring to Claim 18, Wilson in view of Kronberg and in further view of Matsuda disclose the switch matrix circuit of claim 14, Kronberg discloses wherein the transistor further comprises a bipolar junction transistor (column 3 lines 55 to 60; see Figure 1c).

***Allowable Subject Matter***

Claims 27 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claim 27, the following is a statement of reasons for the indication of allowable subject matter: the prior art fail to suggest limitations wherein detecting the switch status of the switch comprises:

Receiving a base current level associated with a low logic state in a selected row of switch matrix, wherein the switch is located at the intersection of the selected row and column;

If the switch is closed, amplifying at least a portion of the base current level conducted by the column to at least the threshold current level with a transistor coupled at its base to the column and at its emitter to a scan line; and

Scanning the scan line for the current signal, wherein the switch status is open if the current signal is less than the threshold current level, and wherein the switch status is closed if the current signal is at least the threshold current level.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bauer (US# 4,673,933) discloses a switch matrix encoding interface using common input/output parts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam V Nguyen whose telephone number is 571-272-3061. The examiner can normally be reached on Mon-Fri, 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached on 571-272-3068. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nam Nguyen
December 2, 2005

MICHAEL HORABIK
SUPERVISORY PATENT EXAMINER
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